IN THE SPECIFICATION:

Please amend the first full paragraph appearing on page 3 as follows:

FIG. 1 is a schematic representation of an exemplary conventional antifuse element 1, which includes a metal contact 2, first and second electrodes 4 and 8, respectively, and a dielectric layer 6, which electrically insulates the first electrode 4 from the second electrode 8. Metal contact 2 is typically a large element relative to the remainder of antifuse element 1. As a current is applied to metal contact 2, the resistance that is generated thereby and by at least one of the electrodes 4, 8 that are in contact therewith locally heats dielectric layer 6, destroying at least a portion of the same and facilitating the formation of an electrically conductive pathway between first electrode 4 and second electrode 8. Thus, an electrical contact is established between first and second electrodes 4 and 8, respectively, thereby activating ~~the antifuse element.~~ antifuse element 1.

Please amend the second full paragraph appearing on page 3 as follows:

As noted previously, programming pulses which comprise high electrical voltages may damage various components of an EEPROM, ~~including without limitation~~ including, without limitation, the gate oxide layer, transistors and other structures on the surface of the EEPROM. Consequently, in order to reduce the potential for damaging EEPROMs during the programming thereof, the programming pulses for EEPROMs are ever-decreasing, as are the normal operating voltages thereof. State of the art EEPROMs typically operate at either 5V or 3.3V. United States Patent 5,486,707, issued to Kevin T. Look et al. on January 23, 1996, discloses an exemplary programmable memory that includes antifuse elements that may be switched to an "on" state by a programming voltage of about 7.5V to about 10V. While in the "off" state, the electrical resistance of a typical EEPROM antifuse element is on the order of about 1 gigaohm or greater. After an antifuse of a typical state of the art EEPROM has been switched to the "on" state by a programming pulse, the former has a low electrical resistance, on the order of tens of ohms or less.

Please amend the paragraph bridging pages 3 and 4 as follows:

The memory elements of such state of the art EEPROMs typically have lower programming voltage requirements than their predecessors, due to the structure of the memory elements of the former and the materials that are utilized in the memory elements. While the programming voltage requirements of such EEPROMs are ~~ever-decreasing,~~ ever-decreasing, due to the widespread use of conventional, low thermal impedance metal contacts in connection with the antifuse elements thereof, an extremely high current is typically required in order to generate a sufficient temperature to activate such antifuse elements. Further, due to the high rate at which many conventional metal contacts dissipate heat, such contacts may necessitate the input of even greater amounts of current in order to adequately heat and activate an antifuse element. Moreover, the typical use of conventional, relatively large metal contacts on such EEPROMs is somewhat undesirable from the standpoint that such contacts consume a great deal of surface area or "real estate" on the surface of the semiconductor device. Thus, conventional metal contacts limit the density of active device regions on the semiconductor device.

Please amend the second full paragraph appearing on page 5 as follows:

The electrical and thermal contact of the present invention addresses each of the foregoing needs. The electrical and thermal contact of the present invention contacts a structure of a semiconductor device, such as a phase change component of an active device region thereof, as disclosed in the '758 ~~Patent,~~ Patent and in United States Patent 5,789,277 ("the '277 Patent"), which issued to Zahorik et al. on August 4, 1998, the disclosures of both of which are hereby incorporated by reference in their entirety. The electrical and thermal contact of the present invention includes an intermediate conductive layer adjacent the contacted structure, a thermal insulator component, which is also referred to as an insulator component, that is adjacent the intermediate conductive layer, and a contact layer that is adjacent the thermal insulator component and which partially contacts the intermediate conductive layer. Preferably, the contact layer and intermediate conductive layer are in electrical and thermal communication with

the contacted structure. The thermal insulator component is preferably sandwiched between the intermediate conductive layer and the contact layer, such that the thermal insulator component is substantially enveloped by the intermediate conductive and contact layers. An exemplary active device region to which the electrical and thermal contact of the present invention may be contacted is a memory cell, or element, of an ~~electrically erasable programmable memory (EEPROM)~~ EEPROM device.

Please amend the paragraph bridging pages 5 and 6 as follows:

Fabricating the electrical and thermal contact includes forming a dielectric layer around the lateral peripheral portions of a semiconductor device structure to be contacted, patterning the dielectric layer to expose at least a portion of the semiconductor device structure to be contacted, such as an active device region thereof, depositing a first thin conductive layer, depositing another dielectric layer adjacent the first thin conductive layer, patterning the dielectric layer to define a thermal insulator component, depositing a second thin conductive layer adjacent the thermal insulator component and in electrical communication with the first thin conductive layer, and patterning the first and second thin conductive layers to define the intermediate conductive layer and the contact layer, respectively. The dielectric layer is fabricated from an electrically and thermally conductive material. Preferably, during patterning of the dielectric layer, the first thin conductive layer is utilized as an etch stop. The processes that may be employed to fabricate the electrical and thermal contact facilitate the fabrication of a relatively small electrical and thermal ~~contact,~~ contact when compared with conventional metal contacts.

Please amend the sixth full paragraph appearing on page 7 as follows:

The present invention comprises an electrical and thermal contact for a contacted structure of a semiconductor device. With reference to FIGs. 2 and 3, in a preferred embodiment, the electrical and thermal contact 10 is disposed on a surface 15 of a semiconductor device 14. Electrical and thermal contact 10 may be positioned adjacent a contacted structure 12, such as an antifuse or other memory element, that is exposed through oxide layer 11, such that it electrically and thermally contacts the contacted structure 12. Preferably, electrical and thermal contact 10

contacts an electrically conductive phase change component 13 of contacted structure 12 (FIG. 3), such as the memory element disclosed in the '758 Patent. Preferably, contacted structure 12 includes a dielectric element 19 surrounding the lateral peripheral portions of phase change component 13 to thermally and electrically insulate the latter.

Please amend the paragraph bridging pages 7 and 8 as follows:

Electrical and thermal contact 10 includes a thin, intermediate conductive layer 16, disposed adjacent contacted structure 12, a thermal insulator component 20 positioned adjacent ~~the intermediate~~ intermediate conductive layer 16, and a thin, electrically conductive contact layer 22 disposed adjacent ~~the thermal~~ thermal insulator component 20. Preferably, thermal insulator component 20 is sandwiched between intermediate conductive layer 16 and contact layer 22, such that thermal insulator component 20 is substantially enveloped by the intermediate and contact layers.

Please amend the first full paragraph appearing on page 8 as follows:

Phase change component 13 is preferably fabricated from an electrically conductive phase change material, such as amorphous silicon or a so-called "chalcogenide" alloy, which typically includes at least one of germanium, antimony, selenium, and ~~telurium.~~ tellurium. Such materials exhibit different electrical characteristics, depending upon their state. For example, phase change materials such as chalcogenides exhibit greater electrical conductivity when in a crystalline phase than in an amorphous phase.

Please amend the second full paragraph appearing on page 8 as follows:

Intermediate conductive layer 16 is positioned such that it electrically contacts phase change component 13 and establishes electrical communication between contact layer 22 and contacted structure 12. Intermediate conductive layer 16 is fabricated from an electrically conductive material and preferably has a thickness of about 200Å or less. Preferably, in order to maintain the structural integrity of intermediate conductive layer 16 during the operation of semiconductor device 14, the material from ~~which the~~ which intermediate conductive layer 16 is

fabricated has a melting point that is higher than both the ambient temperature at ~~which the~~ which semiconductor device 14 operates and the phase change temperature of phase change component 13. An exemplary material that may be used to fabricate intermediate conductive layer 16 is titanium nitride (TiN), which may be deposited in highly conformal layers of about 200Å or less by techniques that are known in the art, such as chemical vapor deposition processes. Other materials that may be used to define intermediate conductive layer 16 include, without limitation, tungsten, titanium, other refractory metals, other refractory metal nitrides, metal alloys and other materials which are useful as electrically conductive traces on semiconductor devices.

Please amend the paragraph bridging pages 8 and 9 as follows:

Thermal insulator component 20 is disposed upon intermediate conductive ~~layer 16,~~ layer 16 and is preferably positioned over contacted structure 12. Thermal insulator component 20 may be fabricated from a thermally insulative material, such as a silicon oxide (e.g., SiO_2), a doped silicon oxide (e.g., borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), borosilicate glass (BSG)), silicon nitride, thermoset resins, thermoplastic polymers, and other dielectric materials which exhibit good thermal insulative properties.

Please amend the first full paragraph appearing on page 9 as follows:

Contact layer 22 is preferably disposed over the entire surface of thermal insulator component 20 and over the exposed portions of intermediate conductive layer 16 that are adjacent ~~to the~~ to thermal insulator component 20. Contact layer 22 is fabricated from an electrically conductive material that preferably has a thickness of about 200Å or less. Preferably, in order to maintain the structural integrity of contact layer 22 during the operation of semiconductor device 14, the material from which the contact layer 22 is fabricated has a melting point that is higher than both the ambient temperature at ~~which the~~ which semiconductor device 14 operates and the phase change temperature of phase change component 13. An exemplary material from which contact layer 22 may be fabricated is titanium nitride (TiN), which may be deposited in highly conformal layers of about 200Å or less by techniques that are

known in the art, such as chemical vapor deposition processes. Alternatively, contact layer 22 may be manufactured from materials including, without limitation, aluminum, tungsten, titanium, other refractory metals, other refractory metal nitrides, metal alloys and other materials that are useful as electrically conductive traces in semiconductor device applications.

Please amend the paragraph bridging pages 9 and 10 as follows:

Referring now to FIG. 4, in order to form intermediate conductive layer 16 (*see* FIGs. 2 and 3), a first thin layer 24 of thermally and electrically conductive material is deposited on surface 15 of semiconductor device 14, such that it contacts portions of phase change component 13 that are exposed ~~through the oxide layer 11 of surface 15~~. First thin layer 24 may be formed by techniques that are known in the art which are capable of depositing an electrically conductive layer formed of a desired material and having a desirable thickness and conformity. Thin-film deposition techniques that are useful for forming first thin layer 24 include, without limitation, chemical vapor deposition (CVD) processes (e.g., ~~atomospheric~~ atmospheric pressure CVD, low pressure CVD, plasma-enhanced CVD) and sputtering, or physical vapor deposition, processes. Such techniques typically blanket-deposit a layer of the desired material over the entire surface of a semiconductor device or larger substrate including a multitude of such devices, including any exposed contacted structures thereof.

Please amend the second full paragraph appearing on page 11 as follows:

The processes that may be employed to fabricate electrical and thermal contact 10 facilitate the fabrication of a structure that is relatively small when compared to the size of conventional metal contacts. Similarly, electrical and thermal contact 10 may be fabricated by processes that form and define structures of various dimensions. The thermal and electrical conductivity of electrical and thermal contact 10 is dependent upon several factors, including, without limitation, the thickness ~~of the~~ of first and second thin layers 24 and 28, the height and mass of the thermal insulator component 20, and various characteristics of the materials from which intermediate conductive layer 16, contact layer 22 and thermal insulator component 20 are fabricated.

Please amend the paragraph bridging pages 11 and 12 as follows:

Referring again to FIG. 3, as noted previously, the disposition of electrical and thermal contact 10 adjacent and in direct contact with phase change component 13 of contacted structure 12 facilitates a reduction in the overall ~~amount~~ amounts of current and heat that are required to operate or ~~activate the~~ activate contacted structure 12 relative to the respective amount of current that is typically required by many semiconductor devices which include conventional heavy electrical contacts over contacted chalcogenide memory elements. Many conventional electrical contacts dissipate substantial amounts of thermal energy into the surrounding ~~environment, and thus~~ environment and, thus, away from the structures in contact therewith.

Please amend the second full paragraph appearing on page 12 as follows:

As current is conveyed through contact layer 22 and intermediate conductive layer 16, thermal energy is created and absorbed by phase change component 13. The long path lengths of layers 16 and 22 provide a high thermal ~~impedence~~ impedance and prevent the heat generated in phase change component 13 from being conducted away from phase change component 13. Thus, phase change component 13 heats to a desirable temperature (e.g., a temperature that will switch phase change component 13 from a first conductivity state to a second conductivity state) with a low voltage input relative to that required by conventional metal contacts.

Please amend the third full paragraph appearing on page 12 as follows:

When phase change component 13 is heated to a sufficient temperature, thermal insulator component 20, which is proximate to phase change component 13, opposite intermediate conductive layer 16, prevents heat from escaping into the environment surrounding electrical and thermal contact 10 and, therefore, prevents heat from escaping phase change component 13.

Please amend the fourth full paragraph appearing on page 12 as follows:

Thus, electrical and thermal contact 10 effectively contains thermal energy within phase change component 13 of contacted structure 12. Moreover, due to its small surface area relative to that of conventional metal contacts, electrical and thermal contact 10 does not dissipate heat as quickly as conventional metal contacts. Thus, the amount of voltage that is required to effect a ~~thermally-induced~~ thermally induced switching of contacted structure 12 from a first state to a second state is also reduced.

Please amend the paragraph bridging pages 12 and 13 as follows:

FIG. 9 illustrates an exemplary use of electrical and thermal contact 10 in an electrically erasable programmable memory semiconductor device 30, which is also referred to as a semiconductor device for simplicity, that includes a plurality of memory elements 32 (although only a single memory element 32 is illustrated in FIG. 9). Exemplary memory elements 32 with which the electrical and thermal contact 10 of the present invention are particularly useful include those disclosed in the '758 Patent. Memory element 32 includes an upper contact electrode 36 and a lower contact electrode 38, both of which may comprise a phase change material. As illustrated, memory element 32 also includes diffusion regions of p-doped isolation channels 39 adjacent lower contact electrode ~~38, and~~ 38 and an n-epitaxial structure 40 adjacent the p-doped isolation channel 39. An n+ channel 41, which addresses the individual memory ~~cells~~ elements 32, is adjacent and in electrical communication with n-epitaxial structure 40. Electrical and thermal contact 10 preferably contacts upper contact electrode 36, which may comprise phase change component 13. Although FIG. 9 illustrates a vertically contacted memory element 32, the electrical and thermal contact 10 of the present invention may also be employed in association with other memory element designs or configurations, as are known to those of skill in the art, as well as with other types of memory devices and other structures that may be fabricated on semiconductor devices and for which an infusion of thermal energy with a reduced, or lower, level of current input may be desired.

Please amend the paragraph bridging pages 13 and 14 as follows:

With continued reference to FIG. 9, as an example of the use of electrical and thermal contact 10 in programming memory element 32, a programming impulse source 42 is placed into electrical contact with contact layer 22. An electrical current generated by programming impulse source 42 is then conducted through contact layer 22 and intermediate conductive layer 16, and through the phase change component 13 thereof, and causes phase change component 13 to change phase, thereby altering the electrical conductivity characteristics of phase change component 13. Thermal insulator component 20 and low thermal conduction of upper contact electrode 36 prevent the escape of heat from memory element 32. Thus, self-heating of the phase change material of phase change component 13, due in part to the resistivity thereof, heats memory element 32 to a temperature that is sufficient to ~~activate the~~ activate memory element 32 and create a low resistance electrical pathway through memory element 32, thereby switching memory element 32 from an "off" state to an "on" state.

Please amend the second full paragraph appearing on page 14 as follows:

Electrical and thermal contact 110, 110′ includes a thin, electrically conductive base layer 116, 116′ disposed on surface 115, 115′ of semiconductor device 114, 114′ and in electrical contact with a first conductive element 130, 130′ of memory element 112, 112′. ~~An~~ A thermal insulator component 120, 120′ of electrical and thermal contact 110, 110′ is disposed on base layer 116, 116′. An electrically conductive contact layer 122, 122′ is disposed adjacent thermal insulator component 120, 120′, and in electrical contact with base layer 116, 116′. Each of the elements of electrical and thermal contact 110, 110′ may be fabricated from the materials and by the processes that were discussed above.

Please amend the fourth full paragraph appearing on page 14 as follows:

As an example of the use of electrical and thermal contact 110, 110′ in programming a memory element 112, 112′, a programming impulse source 142, 142′ is placed into contact with contact layer 122, 122′. An electrical current that is generated by programming impulse source 142, 142′ is then conducted through contact layer 122, 122′ to memory element 112, 112′. Heat

generated in memory element 112, 112′ causes it to switch states. The heat is prevented from leaving the memory element 112, 112′ by the low thermal conductivity of electrical and thermal contact 110, 110′.